

Popis komunikačného protokolu pre ED-5000

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1 Popis protokolu

1.1 Nastavenie komunikačného portu

Prenosová rýchlosť	38400 Bd
Počet dátových bitov	8
Parita	žiadna
Počet stop bitov	1

1.2 Popis komunikácie

Všetky funkcie displeja sú prístupné cez sadu registrov. Zápis do registra vždy pozostáva z prenosu troch bajtov.

Prvý bajt (ADDR) je stále posielaný hostom. Spodných sedem bitov určuje adresu registra, ku ktorému sa bude pristupovať. Najviac významový bit je tzv. R/W (read/write) bit. Ak R/W bit má hodnotu 0, host číta dáta z kontroléra displeja, ak R/W bit má hodnotu 1, host dáta do kontroléra displeja zapisuje.

Druhý bajt (DATA) je dátový bajt a smer jeho prenosu, a teda aj zariadenie, ktoré ho vysielá sú závislé od hodnoty R/W bitu.

Tretí bajt (CRC) je zabezpečovací bajt. Je vždy vysielaný kontrolérom displeja. Jeho hodnota sa vypočítava exkluzívnym súčtom (XOR) prvého a druhého bajtu a hodnoty 0x0f.

Tabuľka 1. Formát prvého bajtu (ADDR)

7	6	5	4	3	2	1	0
R/W	Adresa registra						

Tabuľka 2. Zápis do registra

PC	smer prenosu	ED-5000
ADDR	->	
DATA	->	
	<-	CRC ¹⁾

Poznámka

¹⁾ CRC = ADDR xor DATA xor 0x0F

Tabuľka 3. Čítanie registra

PC	smer prenosu	ED-5000
ADDR	->	
	<-	DATA
	<-	CRC ¹⁾

Poznámka

¹⁾ CRC = ADDR xor DATA xor 0x0F

2 Organizácia zobrazovacej časti displeja

Základom je displej s 2 x 20 znakmi, ktorý je rozdelený na tri rôzne zobrazovacie oblasti.

Rozmery prvej oblasti sú identické s rozmermi prvého riadku displeja, t.z. 1 riadok x 20 znakov. Tejto oblasti zodpovedá skupina registrov CHRA00 - CHRA19 (prístupné sú na adresách 0x30 - 0x43). Druhá a tretia zobrazovacia oblasť tvoria druhý riadok displeja. Druhá zobrazovacia oblasť je tvorená šiestimi znakmi, ktorým zodpovedajú registre CHRB00 - CHRB05 (adresy 0x44 - 0x49) a tretiu oblasť tvorí desať znakov. Tie sú prístupné prostredníctvom registrov CHRB06 - CHRB15 (adresy 0x4a - 0x53). Zostávajúce štyri znaky sú prístupné cez registre CHRB16 - CHRB19 (adresy 0x54 - 0x57). Tieto znaky nie sú však na displeji viditeľné.

3 Display Registers

3.1 Introduction

This section describes Registers of Euro Displays. Euro Display presents two rows (or lines) of characters arranged in two groups. Each group contains twenty characters. Physical device can contain all, or subset of these characters. Device driver is responsible for mapping existing character on physical device to Euro Display character register. Displayed pattern of any character creates matrix of pixels with 8 rows and 5 columns.

Registers are elements of display unit which keep eight bit values. These values can control display unit.

Document specifies basic capabilities and functions of registers. Such description is useful for realization of services which display device driver should provide.

3.2 Register Description

Display registers allow basic control of the display unit. Any Display Register is represented by its name, address and contains value. Register Write and Register Read Operation are defined with their impact on display unit behavior. In the next Display Registers are listed and described.

Table 1. Registers Summary

Name	Abbreviation	Access	Initial Value	Address
Character Register <i>gc</i>	CHRGc	Read/Write	32 (0x20)	48 (0x30) - 87 (0x57)
Glyph Code Register	GCR	Read/Write	0	88 (0x58)
Glyph Value Register	GVR	Write Only	0	89 (0x59)
Backlight Control Register	BLCR	Read/Write	0	40 (0x2C)
Cursor Position Register	CPR	Read/Write	0	41 (0x2D)
Cursor Type Register	CTR	Read/Write	0	42 (0x2E)
Display Control Register	DCR	Read/Write	0	43 (0x2F)
Firmware Version Register	FVR <i>i</i>	Read Only	CHARACTER _i ¹⁾	0 (0x00) - 15 (0x0F)

User Defined Register	UDR	Read/Write	0	90 (0x5A)
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Note

¹⁾ CHARACTER_i is a character code with index 'i' from Firmware Version String

Access to Register addressed outside the ranges shown in Table 1. leads to unpredictable results.

3.3 Character Register (CHRGc)

Register CHRGc value is displayed as character in the group *g* and column *c* of the display unit while display is enabled (see DCR). Dot matrices of displayed characters are shown on the page 6 of the document Standard Character Pattern (KS0066UP-24). There are two groups of Character Registers: A, B. Write Operation in register changes displayed character and Read Operation returns character code of displayed unit without regard on DCR value. CPR value is not affected.

Table 2. Character Register Details

Register Address	Address Value	Register Content
CHRA00	48 (0x30)	code of the character at group A and column 0
CHRA01	49 (0x31)	code of the character at group A and column 1
CHRA02	50 (0x32)	code of the character at group A and column 2
CHRA03	51 (0x33)	code of the character at group A and column 3
CHRA04	52 (0x34)	code of the character at group A and column 4
CHRA05	53 (0x35)	code of the character at group A and column 5
CHRA06	54 (0x36)	code of the character at group A and column 6
CHRA07	55 (0x37)	code of the character at group A and column 7
CHRA08	56 (0x38)	code of the character at group A and column 8
CHRA09	57 (0x39)	code of the character at group A and column 9
CHRA10	58 (0x3A)	code of the character at group A and column 10
CHRA11	59 (0x3B)	code of the character at group A and column 11
CHRA12	60 (0x3C)	code of the character at group A and column 12
CHRA13	61 (0x3D)	code of the character at group A and column 13
CHRA14	62 (0x3E)	code of the character at group A and column 14
CHRA15	63 (0x3F)	code of the character at group A and column 15
CHRA16	64 (0x40)	code of the character at group A and column 16
CHRA17	65 (0x41)	code of the character at group A and column 17
CHRA18	66 (0x42)	code of the character at group A and column 18
CHRA19	67 (0x43)	code of the character at group A and column 19
CHRB00	68 (0x44)	code of the character at group B and column 0
CHRB01	69 (0x45)	code of the character at group B and column 1
CHRB02	70 (0x46)	code of the character at group B and column 2
CHRB03	71 (0x47)	code of the character at group B and column 3
CHRB04	72 (0x48)	code of the character at group B and column 4

CHRB05	73 (0x49)	code of the character at group B and column 5
CHRB06	74 (0x4A)	code of the character at group B and column 6
CHRB07	75 (0x4B)	code of the character at group B and column 7
CHRB08	76 (0x4C)	code of the character at group B and column 8
CHRB09	77 (0x4D)	code of the character at group B and column 9
CHRB10	78 (0x4E)	code of the character at group B and column 10
CHRB11	79 (0x4F)	code of the character at group B and column 11
CHRB12	80 (0x50)	code of the character at group B and column 12
CHRB13	81 (0x51)	code of the character at group B and column 13
CHRB14	82 (0x52)	code of the character at group B and column 14
CHRB15	83 (0x53)	code of the character at group B and column 15
CHRB16	84 (0x54)	code of the character at group B and column 16
CHRB17	85 (0x55)	code of the character at group B and column 17
CHRB18	86 (0x56)	code of the character at group B and column 18
CHRB19	87 (0x57)	code of the character at group B and column 19

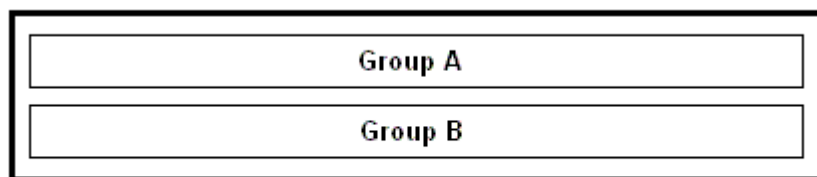
Table 3. CHRgc

Bit	7	6	5	4	3	2	1	0
	CHARACTER CODE ¹⁾							
Initial Value	0x20							
Access	Read / Write							

Note

¹⁾ CHARACTER CODE from device unit code page is in range from 0 to 0xFF. Displayed patterns of codes 0 to 7 are changeable using Glyph Value Register (GVR) Write operation.

Disposition of Euro Display characters is shown on the next picture.

**Figure 1. Display groups arrangement****3.4 Glyph Code Register (GCR)**

Value of GCR selects one character code from display code page which glyph (displayed pattern of this code) can be changed. Glyph of CHARACTER CODE range from 0 to 7 can be defined only (lower eight character codes of display code page). It means that valid value of GCR is from range 0 to 7. Glyph code selection is allowed when BUSY flag is low (0). Writing into GCR when BUSY is true leads to unpredictable results. Glyph pixels can be changed with Write Operation into Glyph Value Register (GVR).

GCR address is 88 (0x58).

Table 4. GCR

Bit	7	6	5	4	3	2	1	0
	BUSY ¹⁾					CHARACTER CODE ²⁾		
Initial Value	0					0		
Access	Read Only		_3)	_3)	_3)	_3)	Read / Write	

Note

¹⁾ BUSY flag when true indicates that display unit changes some glyph matrix , so neither glyph code nor glyph values should be written while Busy is true.

²⁾ Glyph of CHARACTER CODE (value from 0 to 7) can be changed using Glyph Value Register (GVR) Write operation.

³⁾ Access to the bit is not defined

3.5 Glyph Value Register (GVR)

Glyph is formed as pixel matrix with 8 rows and 5 columns. GVR encodes one row of that matrix. Bits 7,6,5 hold value of row (ROW = 0 - 7) and any bit 4,3,2,1,0 contains pixel values from columns 4,3,2,1,0. One write operation on GVR changes all pixels on given ROW from leftmost pixel PXL4 to rightmost pixel PXL0. GVR can be written only in case GCR BUSY flag is false. Code value of affected glyph is taken from current value of Glyph Code Register (GCR).

GVR address is 89 (0x59).

Table 5. GVR

Bit	7	6	5	4	3	2	1	0
	ROW ¹⁾			PXL4 ²⁾	PXL3 ²⁾	PXL2 ²⁾	PXL1 ²⁾	PXL0 ²⁾
Initial Value	0			0	0	0	0	0
Access	Write only			W	W	W	W	W

Note

¹⁾ ROW is a glyph row number value (from 0 to 7)

²⁾ PXL4, PXL3, PXL2, PXL1, PXL0 are pixel element values in row ROW of glyph matrix displayed from left to right

3.6 Backlight Control Register (BLCR)

The lowest bit of this register controls display full brightness backlight. Bits 1 to 7 contains brightness value in percent. Writing high into bit 0 switches display backlight to full brightness. If this bit is low, backlight brightness depends on value in bits 1 to 7. Backlight status is returned from Read BLCR operation.

BLCR address is 40 (0x2C).

Table 6. BLCR

Bit	7	6	5	4	3	2	1	0
	BRIGHTNESS							BL

Initial Value	0	0
Access	Read/Write	Read/Write

3.7 Cursor Position Register (CPR)

Display cursor position can be controlled using CPR. Bits 7 and 6 hold encoded CURSOR GROUP position and bits 5 - 0 hold CURSOR COLUMN position. For Euro Display CURSOR GROUP value is from 0 to 1. Value 0 encodes group A and 1 is for group B. Valid CURSOR COLUMN value is from 0 to 19 for both groups. Using values outside these ranges can lead to unpredictable results. Write Operation into any Character Register (CHRGc) does not change CPR value.

CPR address is 41 (0x2D).

Table 7. CPR

Bit	7	6	5	4	3	2	1	0
	CURSOR GROUP		CURSOR COLUMN					
Initial Value	0		0					
Access	Read/Write		Read/Write					

3.8 Cursor Type Register (CTR)

Bits 1 and 0 of this register controls cursor state and character blinking. Writing value 1 into the BLINK bit causes periodical changing black space and character on the same place. Position of blinked character is given in Cursor Position Register (CPR). Writing value 1 into the CURSOR bit displays cursor as lowest pattern matrix line (underline character). Writing low value into the CURSOR bit switches cursor off. Blinking and cursor states are returned from CTR Read Operation.

CTR address is 42 (0x2E).

Table 8. CTR

Bit	7	6	5	4	3	2	1	0
							CURSOR	BLINK
Initial Value							0	0
Access	_1)	_1)	_1)	_1)	_1)	_1)	Read/Write	Read/Write

Note

¹⁾ Access to the bit is not defined

Table 9.

CURSOR	BLINK	Effect on Cursor Position
0	0	character is displayed
0	1	character and black box are interlaced
1	0	character with underline is displayed

1	1	underlined character and black box are interlaced
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3.9 Display Control Register (DCR)

The lowest bit of this register controls displaying of all columns and rows. Writing high value into DE bit of DCR displays all characters as they are written in the CHRgc. Writing low value into DE bit of DCR causes white spaces are displayed. Display Enable status is returned from Read DCR operation.

High value written in bit POWER DOWN causes transition to display power down state. Display leaves this low power consuming state when any Register is accessed and POWER DOWN is cleared. Consecutive reading of bit POWER DOWN after setting it to "1" has no sense, because this wakes up display at once. Only writting "1" is meaningful for POWER DOWN bit and activates transition into power down state.

Activating bit CLEAR (writting "1" into it) clears display. White spaces are then displayed and cursor is moved at begin. At the end of clear activity display resets bit CLEAR to "0". No display control command is allowed till CLEAR is on level "1" and clear sequence in display continues.

DCR address is 43 (0x2F).

Table 10. DCR

Bit	7	6	5	4	3	2	1	0
						CLEAR	POWER DOWN	DE ¹⁾
Initial Value						0	0	0
Access	_2)	_2)	_2)	_2)	_2)	Read/Write	Read ^{3)/} Write	Read/Write

Note

1) DE controls display switching on/off in Write Operation and is returned in Read Operation as display enable status.

2) Access to the bit is not defined.

3) Write only operation is meaningful. Any attempt to read DCR (or acces another Register) after setting POWER DOWN on "1" returns display back in powered state.

3.10 Firmware Version Register (FVRi)

In registers FVR00, FVR01, ..., FVR15 is stored firmware version string which identifies current display unit firmware version. The string is encoded in UTF-8 form and contains codes from U+0020 to U+007D. The first character of the string is in FVR00. Maximal string length is 16. In this case the last character of the string is in FVR15. If version string has a shorter length 'L' (L < 16) then FVRL to FVR15 values are 0 (ending zeroes).

Table 11. Firmware Version Register Details

Register Address	Address Value
FVR00	0 (0x00)
FVR01	1 (0x01)
FVR02	2 (0x02)
FVR03	3 (0x03)

FVR04	4 (0x04)
FVR05	5 (0x05)
FVR06	6 (0x06)
FVR07	7 (0x07)
FVR08	8 (0x08)
FVR09	9 (0x09)
FVR10	10 (0x0A)
FVR11	11 (0x0B)
FVR12	12 (0x0C)
FVR13	13 (0x0D)
FVR14	14 (0x0E)
FVR15	15 (0x0F)

Table 12. FVR*i*

Bit	7	6	5	4	3	2	1	0
Initial Value	CHARACTER _{<i>i</i>} ¹⁾							
Access	Read Only							

Note

¹⁾ CHARACTER_{*i*} is a character code from Firmware Version String on position 'i' (0 ≤ *i* < 16).

3.11 User Defined Register (UDR)

UDR holds value previously written by Register Write operation and does not change it. UDR content is returned by Display Read operation. On display initialization this value is cleared to 0x00.

UDR address is 90 (0x5A).

Table 13. UDR

Bit	7	6	5	4	3	2	1	0
	USER VALUE							
Initial Value	0x00							
Access	Read / Write							

4 Znaková sada kontroléra displeja (KS0066UP-24)

Upper 4bit Lower 4bit		LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)																
LLLH	(2)																
LLHL	(3)																
LLHH	(4)																
LHLL	(5)																
LHLH	(6)																
LHHL	(7)																
LHHH	(8)																
HLLL	(1)																
HLLH	(2)																
HLHL	(3)																
HLHH	(4)																
HHLL	(5)																
HHLH	(6)																
HHHL	(7)																
HHHH	(8)																